

ABSTRACT OF THE DISCLOSURE

The image processor comprises a switch that divides image data into  $m \times n$  pixels, having  $n$  lines with  $m$  pixels per one line; a group of line memories that store the divided image; a compression device which batch compresses the image data of  $m \times n$  pixels. Further, a command control unit provides control so as to send the  $(n-1)$  lines of image data among  $m \times n$  pixels of image data to the group of line memories, and the remaining one line of image data directly to the compression device 902, and to send the  $m \times (n-1)$  pixels of image data stored in the line memories to the compression device.